Application Note

NOVOSENSE

EMC Circuit of NSPASx

AN-12-0001

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ABSTRACT

This application note introduces 3 different application circuits of NSPASx series with different levels of EMC performance. According to the EMC requirement, one of the circuits could be used as a reference in application and minor modification could be done based on the original circuit. NSPASx stands for NSPAS3, NSPAS3M & NSPAS1 with the same ASIC inside different packages.

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1.Hardware

1.1. General edition

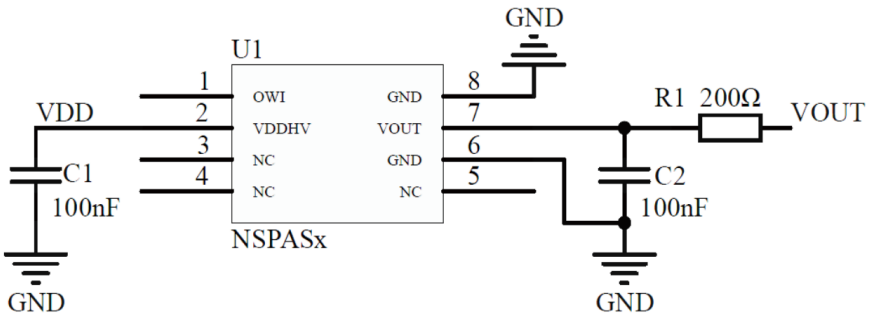

Figure 1. Typical application circuit

1.1.1.EMC performance

Items	Standards	Test	Severity
Radiated Immunity (ALSE Method)	ISO 11452-2：2004	100V/m	Class C
Bulk current injection (BCI)	ISO 11452-4：2011	100mA	Class C
ESD (Contact /Power off)	ISO 10605：2008	8KV	Class A <100mV

*ESD HBM 2000Ω/330pF

1.2.EMI enhanced edition

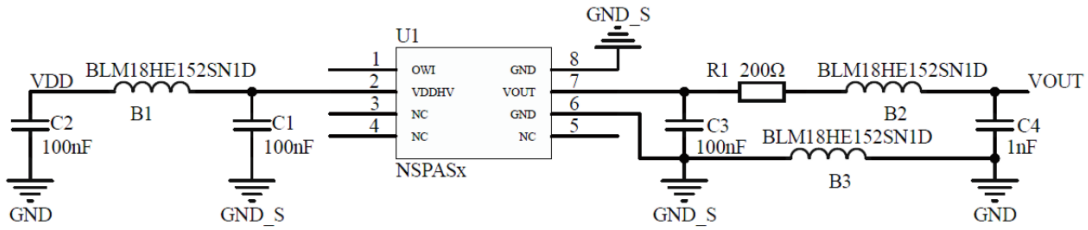

Figure 2. EMI enhanced application circuit

1.2.1.EMC performance

Items	Standards	Test	Severity
Radiated Immunity (ALSE Method)	ISO 11452-2：2004	100V/m	Class A <100mV
Bulk current injection (BCI)	ISO 11452-4：2011	100mA	Class A <100mV
ESD (Contact /Power off)	ISO 10605：2008	8KV	Class A <100mV

*ESD HBM 2000Ω/330pF

1.3.EMI & ESD enhanced edition

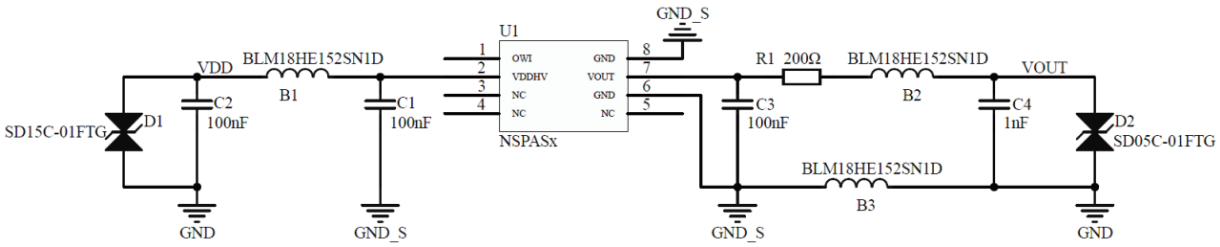

Figure 3. EMI & ESD enhanced application circuit

1.3.1.EMC performance

Items	Standards	Test	Severity
Radiated Immunity (ALSE Method)	ISO 11452-2：2004	100V/m	Class A <100mV
Bulk current injection (BCI)	ISO 11452-4：2011	100mA	Class A <100mV
ESD (Contact /Power off)	ISO 10605：2008	16KV	Class A <100mV

*ESD HBM 330Ω/330pF

2.BOM

Comment	Designator	Footprint	Value
TVS	D1	1608	SD15C-01FTG
TVS	D2	1608	SD05C-01FTG
Bead	B1	1005	BLM18HE152SN1
Bead	B2	1005	BLM18HE152SN1
Bead	B3	1005	BLM18HE152SN1
Cap	C1	1608	100nF
Cap	C2	1608	100nF
Cap	C3	1608	100nF
Cap	C4	1608	1nF
Resistor	R1	1608	200Ω
NSPASx	U1	SOP8	

3.Layout

The TVS protects the VDDHV and OUT pins from damage caused by transient high voltage pulses. If the applied EMC environment is harsh, can replace the TVS with higher power at the expense of a larger package size. On the PCB layout, it is necessary to place the two TVS as close as possible to the connector.

The C1 capacitor filters out power supply noise and keeps the power supply input stable. Place this capacitor as close to the U1 VDDHV pins as possible. The power line first passes through the capacitor before reaching the chip pins. Similarly, C4 capacitor filters out noise signal from the signal line and keeps the output signal stable which should be placed as close as possible to the output connector.

The beads suppress the noise signal from the power & signal lines during bulk current injection test which should be placed as close as possible to the connectors directly connected to the power & signal lines.

Figure 4 demonstrates one PCB layout example of EMI & ESD enhanced application circuit for NSPAS3.

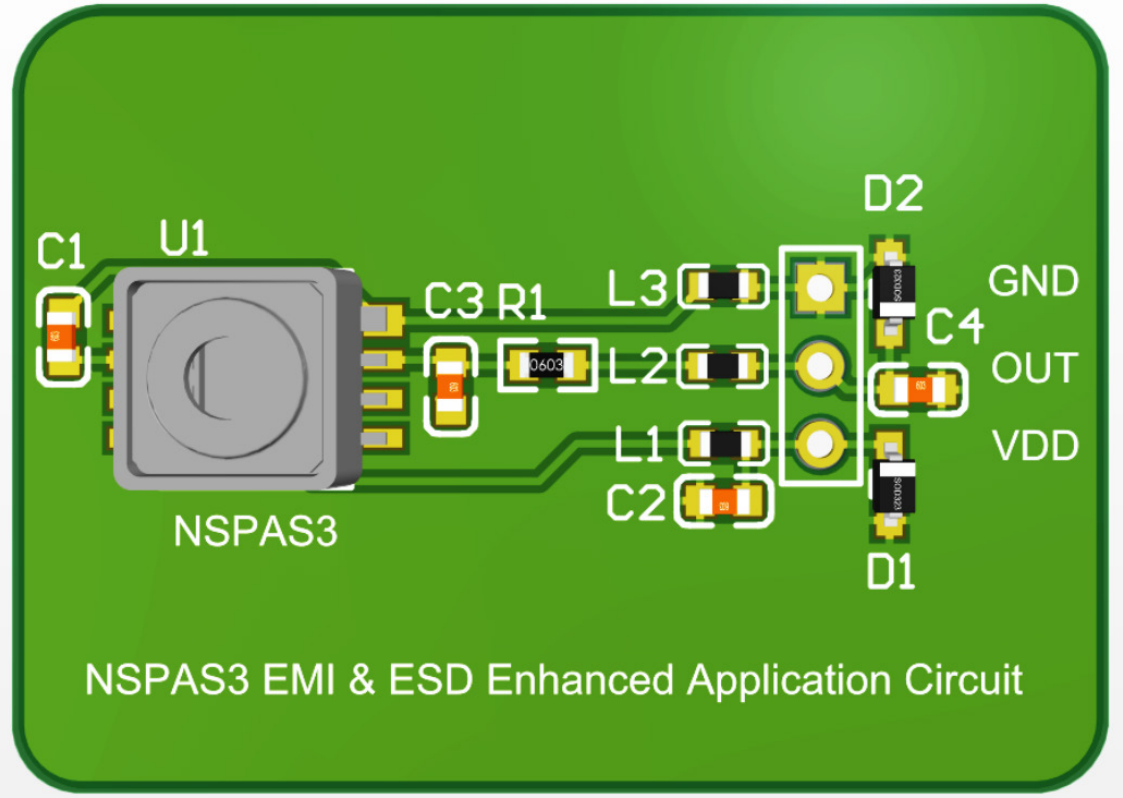

Figure 4. EMI & ESD enhanced application circuit PCB layout

4.Test photos

Figure 5. Radiated Immunity(ALSE Method) 400MHz-1000MHz Vertical

Figure 6. Radiated Immunity(ALSE Method) 1000MHz-2000MHz Horizontal

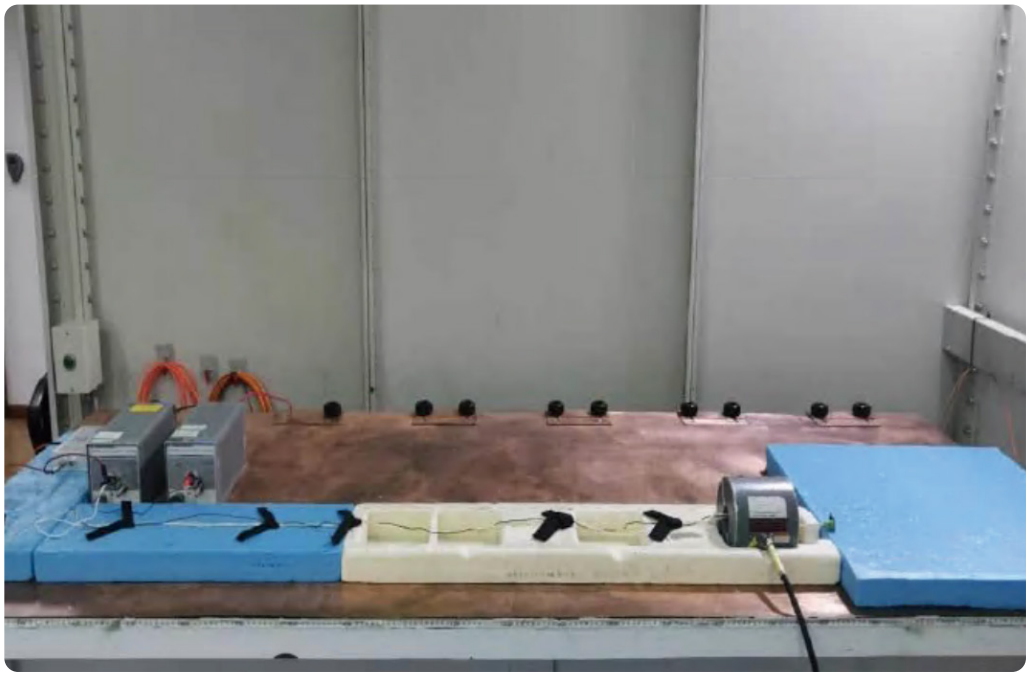

Figure 7. Bulk Current Immunity (CBCI) 15cm

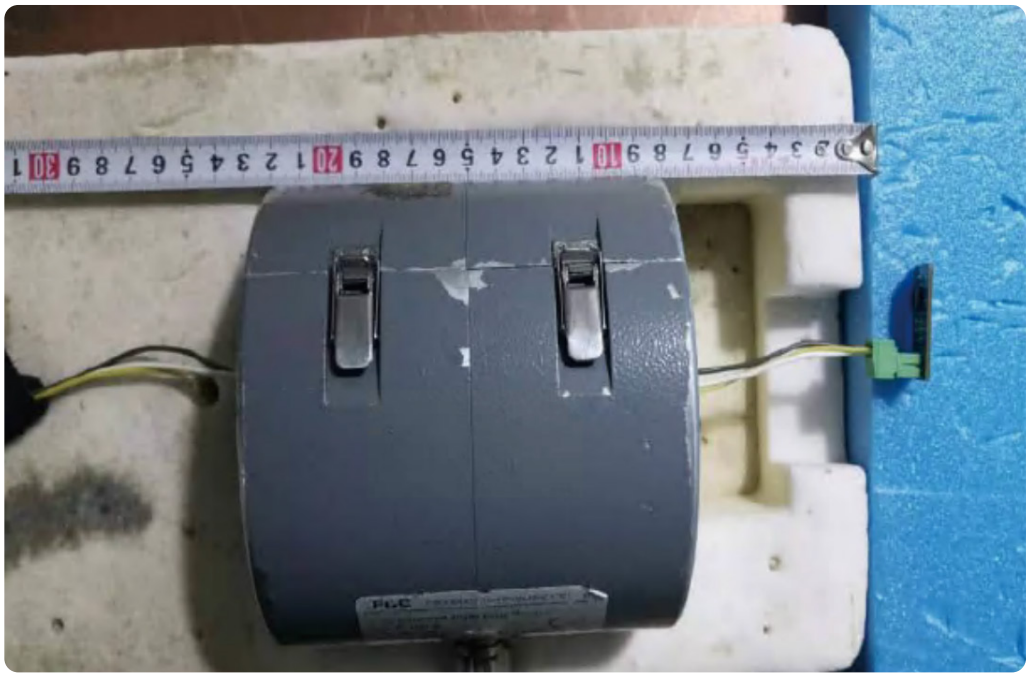

Figure 8. Bulk Current Immunity (CBCI) 15cm

Figure 9. Electrostatic Discharge Unpowered Mode

5.Function performance status classification

Class	Description
Class A	The DUT can perform all its pre-designed functions during and after the interference is applied. The tolerances caused by the disturbance are within the design error range of the DUT.
Class B	During interference, the device under test can perform all its pre-designed functions; however, one or more indicators exceed the specified deviation. All functions automatically return to the normal working range after stopping the interference.
Class C	During interference, the DUT does not perform one or more of its pre-designed functions, which affects the normal operation of the basic functions of the entire system, but it can automatically return to normal operation after stopping the application of interference.
Class D	The DUT does not perform one or more of its pre-designed functions during the application of interference. It will not automatically return to its normal operating state until the application of interference is stopped and a simple "operation or use" reset action is performed.
Class E	During and after the interference is applied, the device under test does not perform one or more of its pre-designed functions, and if it does not repair or replace the device or system, it cannot resume its normal operation.

6.Revision history

Revision	Description	Author	Date
1.0	Initial version	Charles Chen	2023/08/14